Suspended Nanochannel Resonator Arrays with piezoresistive sensors for high-throughput weighing of nanoparticles in solution

Supporting Information.

Marco Gagino†‡#¤Δ, Georgios Katsikis†Δ, Selim Olcum†⊥⁑, Leopold Virot‡⁑, Martine Cochet‡, Aurélie Thuaire‡, Scott R. Manalis†§||, Vincent Agache†‡**

* Corresponding authors

Δ Those co-authors contributed equally

⁑ Those co-authors contributed equally

AUTHOR ADDRESS

† Koch Institute for Integrative Cancer Research, Massachusetts Institute of Technology, Cambridge, MA, USA

‡ Université Grenoble Alpes, CEA, LETI, 38000 Grenoble, France

Politecnico di Torino, Torino, Italy

¤Institut polytechnique de Grenoble, France

§ Department of Biological Engineering, Massachusetts Institute of Technology, Cambridge, MA, USA

|| Department of Mechanical Engineering, Massachusetts Institute of Technology, Cambridge, MA, USA

⊥ Travera, 700 North, Main St, Cambridge MA 02139

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Supporting Information 1: Nomenclature

L	SNR length	α	Hooge's factor
W	SNR width	β^*	Process dependent sensitivity factor
t	SNR thickness	γ	Extra resistance factor due to contacts and traces
w_c	Channel width	π_l	p-type piezoresistivity factor along <100> direction
t_c	Channel thickness	R_S	Sheet resistance (Ohm/square)
t_{LID}	Lid thickness	N_z	Total number of carriers per unit area
w_{ext}	External wall width separating the embedded channel to the SNR sidewalls	N_p	Dopant concentration (per cc)
w_{int}	Internal wall width separating the embedded channel legs	L_c	Embedded channel length
L_{PZR}	Piezoresistor length	E	Young's modulus of silicon
W_{PZR}	Piezoresistor width	ρ_{Si}	Density of silicon
t_{PZR}	Piezoresistor thickness (~ junction depth)	ρ_{water}	Density of water
k	Stiffness	R_x	Displacement sensitivity of the piezoresistor (V/m)
m_{eff}	Effective mass	R_m	Mass sensitivity of the cantilever (mHz/ag)
x_c	RMS vibration amplitude	k_B	Boltzmann constant
f_r	Resonant frequency	T	Cantilever temperature
ω_r	Angular resonant frequency	V_b	Piezoresistor bias voltage
Q	Quality factor	BW	Measurement bandwidth
R_{PZR}	Piezoresistance value	$T_{transit}$	Transit time

Supporting Information 2: SNR design optimization

The design optimization and parametric study have been carried out by accounting for the different noise sources arising from the piezoresistor readout (Johnson, Hooge noise) and the thermomechanical noise of the hollow cantilever. As a starting point, *Piezo D* code[1] has been modified to account for the SNR geometry, resonant frequency, effective mass, stiffness and mass sensitivity. We also account for technological manufacturing constraints which define some boundaries for the SNR geometry. We assume a given resonant frequency target, f_r. Lastly, we utilize a frequency noise goal optimization function which is converted into equivalent mass noise assuming the SNR is driven at the onset of nonlinearity. As a result, the root mean square vibration amplitude is defined by[2]

$$< x_c > = 5.46 \frac{L}{\sqrt{2Q}} \qquad \text{Equation 1}$$

where L is length of the cantilever and Q its mechanical quality factor. Thus, for a given measurement bandwidth BW, and accounting for the boundaries the SNR, its characteristics including the piezoresistor geometry and doping parameters, are adjusted to minimize the frequency noise, with a mean square value defined as

$$\langle \delta\omega^2 \rangle = \frac{k_B T \omega_r BW}{k \langle x_c^2 \rangle Q} + \frac{1}{R_x^2} \frac{\alpha V_b^2 BW^2}{4 \langle x_c^2 \rangle L_{PZR} W_{PZR} N_z} + \frac{1}{R_x^2} \frac{8 k_B T R_S L_{PZR} BW^3}{3 \langle x_c^2 \rangle W_{PZR}} \qquad \text{Equation 2}$$

The first term represents the thermomechanical noise, the second term represents the Hooge's (1/f) voltage noise and the last term represents the Johnson's (white) voltage noise. Here k_B is the Boltzman constant, T the cantilever temperature and ω_r, k, Q are the angular resonant frequency, stiffness and the quality factor of the resonator, respectively. α is the Hooge's parameter, V_b is the bias voltage applied to the piezoresistor, N_z is the total number of carriers, L_{PZR} and W_{PZR} are the

length and width of the piezoresistor. R_S is the sheet resistance (Ohms/square), and finally R_x (V/m) is the piezoresistor sensitivity to displacement, which is defined in[3] by:

$$R_x = V_b \gamma \, \beta^* \frac{3Et(L-0.5L_{PZR})\pi_l}{8L^3} \qquad \text{Equation 3}$$

Here γ is a geometry factor defined as the ratio of the resistance of the strained region in the piezoresistor to the total resistance including unstrained regions, interconnects, and contact pads. β^* defines the piezoresistor efficiency and depends on fabrication parameters, t and L are the cantilever thickness and length and E and π_l are the Young's modulus and maximum longitudinal piezoresistivity of silicon in the <110> direction for p-type piezoresistors.

Finally, the mean square of mass-equivalent noise is given by:

$$\langle \delta m^2 \rangle = \frac{\langle \delta \omega^2 \rangle}{R_m^2} = \langle \delta \omega^2 \rangle \left(\frac{2m_{eff}}{\omega_r} \right)^2 \qquad \text{Equation 4}$$

where m_{eff} is the effective mass of the hollow cantilever (which is a fraction of the total mass[4]), and R_m its mass sensitivity of the cantilever (mHz/ag). The effective mass is given by:

$$m_{eff} = 0.25 \times \left[\begin{array}{c} \rho_{Si} L \times W(2t_{lid} + t_c) + \\ (\rho_{water} - \rho_{Si}) w_c t_c \left(\pi(w_c + w_{int}) + 2\left(L_c - \frac{w_{int}}{2} - w_c \right) \right) \end{array} \right] \qquad \text{Equation 5}$$

where ρ_{Si} and ρ_{water} the density of the silicon and water respectively.

We use the equations above to calculate the mass-equivalent noise of a SNR. The optimization code operates by using a set of boundary conditions for the dimensions and process conditions and a second set of performance constraints. Using the boundary conditions and performance constraints, the code finds the SNR design parameters that results in the lowest mass-equivalent

noise δm. **Table S1** provides the boundary conditions, performance constraints and design parameters.

Design parameters	Boundary conditions	Performance constraints	Constants
L	$700\ nm < t_c < 1\ \mu m$	f_r	$\Delta f = 200$ Hz
w_c	$700\ nm < w_c < 2\ \mu m$	Max temp rise < 4 ºC	Boron dopant
t_c	$500\ nm < w_{ext}, w_{int}$		$Q = 1000$
t_{LID}	$200\ nm < t_{LID}$		$t = 2t_{LID} + t_c$
w_{int}, w_{ext}	$t_{pzr}/t_{LID} < 1/2$		$W = 2w_c + 2w_{ext} + w_{int}$
L_{PZR}	$10^{17} < N_p < 10^{20}$		$W_{PZR} = (w - w_{int})/2$
t_{PZR}	$V_b < 5$		

Table S1: Boundary conditions, performance constraints and constants defined for design optimization of SNRs.

After running the optimization algorithm for resonant frequency targets of 1.5, and 2.5 MHz, the SNR design parameters shown in Table S2 are achieved.

f_r (MHz)	0.5	1.5	2.5
δm (ag)	2.8132	0.712094	0.375984
δm_{th} (ag)	2.81136	0.71192	0.375926
l (μm)	55.9	32.3	25
w (μm)	2.9	2.9	2.9
t (μm)	1.1	1.1	1.1
w_c(μm)	0.7	0.7	0.7
t_c(μm)	0.7	0.7	0.7
w_{ext}, w_{int}(μm)	0.5, 0.5	0.5, 0.5	0.5, 0.5
t_{lid}(μm)	0.2	0.2	0.2
L_{PZR}(μm)	16	10.5	8.6
W_{PZR}(μm)	1.2	1.2	1.2
t_{PZR}(μm)	0.1	0.1	0.1
R_P (kΩ)	6.45	5.4	5.01
N_p (10^{19} per cc)	5.4	4.2	3.8
R_S (Ohm/sq)	218.4	270	299.4
V_b (V)	0.6	0.4	0.3
P_d (μW)	12.8	6.4	4.6
T_{rise} (degree C)	0.37	0.14	0.09

Table S2: SNR devices optimized for resonant frequency targets of 1.5, and 2.5 MHz, accounting for boundary conditions, performance constraints and constants defined in **Table S1**.

	SNR0	SNR1	A1 #10	SNR subsequent generation channel 2x2 μm²
f_r (MHz)	1.5	2.5	2.5	2.5
δm (ag)	0.941656	0.474646	0.404204	0.510544
δm_{th} (ag)	0.941407	0.474569	0.404136	0.510362
l (μm)	31.6	24.3	25.1	35.7
w (μm)	4.5	3.9	3.5	5
t (μm)	1.1	1.1	1.1	2.4
w_c(μm)	1	0.7	1	2
t_c(μm)	0.7	0.7	0.7	2
w_{ext}, w_{int}(μm)	1, 0.5	1, 0.5	0.5, 0.5	0.25, 0.25
t_{lid}(μm)	0.2	0.2	0.2	0.2
L_{PZR}(μm)	11.6	9.1	9.1	18.9
W_{PZR}(μm)	2	1.7	1.5	2.3
t_{PZR}(μm)	0.1	0.1	0.1	0.1
R_P (kΩ)	4.66	4.55	4.72	2.66
N_p (10^{19} per cc)	3.2	3.1	3.4	7.3
R_S (Ohm/sq)	339.4	353.1	329.3	126.7
V_b (V)	0.4	0.3	0.3	0.5
P_d (μW)	8.5	5.5	5.3	26.3
T_{rise} (degree C)	0.16	0.1	0.1	0.41

Table S3: SNR devices optimized for resonant frequency targets of 1.5 MHz, 2.5 MHz, accounting for boundary conditions, performance constraints and constants defined in **Table S1**.

To get as close as possible to the optimum doping concentration for the piezoresistor, a set of ion implantation conditions have been simulated using Silvaco Athena tool. The ion implantation

process simulation takes into account the screen oxide layer used for implantation (10 nm thick). The simulations were done using Monte Carlo model, considering the p-type (Boron) piezoresistor doping with energies of [3, 4, 5] keV and doses of [$5x10^{14}$, $6x10^{14}$, $7x10^{14}$, $8x10^{14}$, $9x10^{14}$, $1x10^{15}$, $2x10^{15}$, $3x10^{15}$] at/cm². As an example, for the SNR#10 of Array A1, the mass-equivalent noise of the SNR has been calculated using the simulated doping profiles for the piezoresistor and is shown on **Figure S1**.

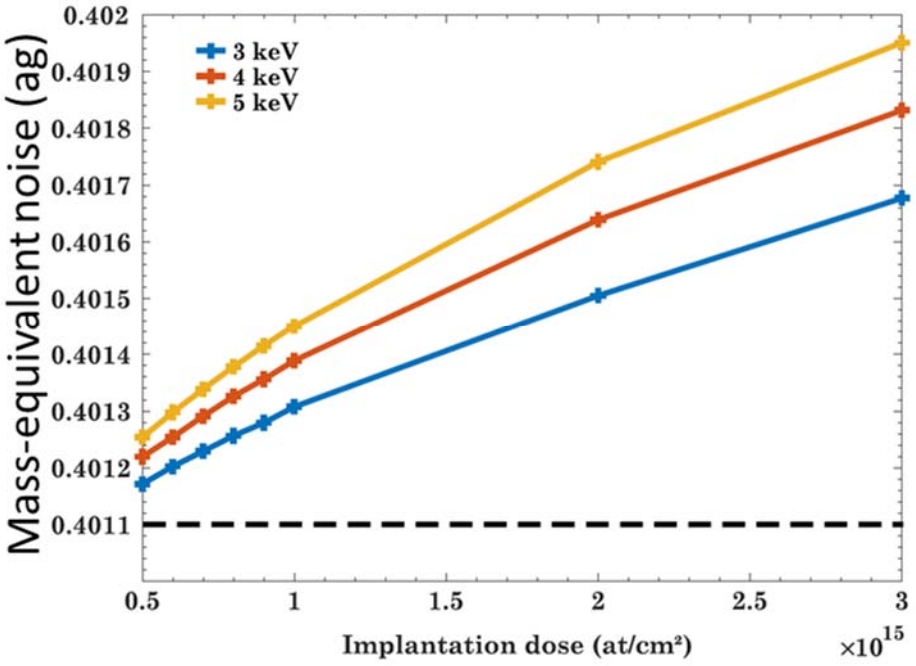

Figure S1. Mass-equivalent noise of a resonator in the parallel SNR array (SNR#10, in A1) vs p-dopant ion implantation dose and energy. The SILVACO simulation takes into account the presence of a 10 *nm*-thick screen oxide layer used during the implantation steps. The dashed line represents the thermomechanical limit for this device.

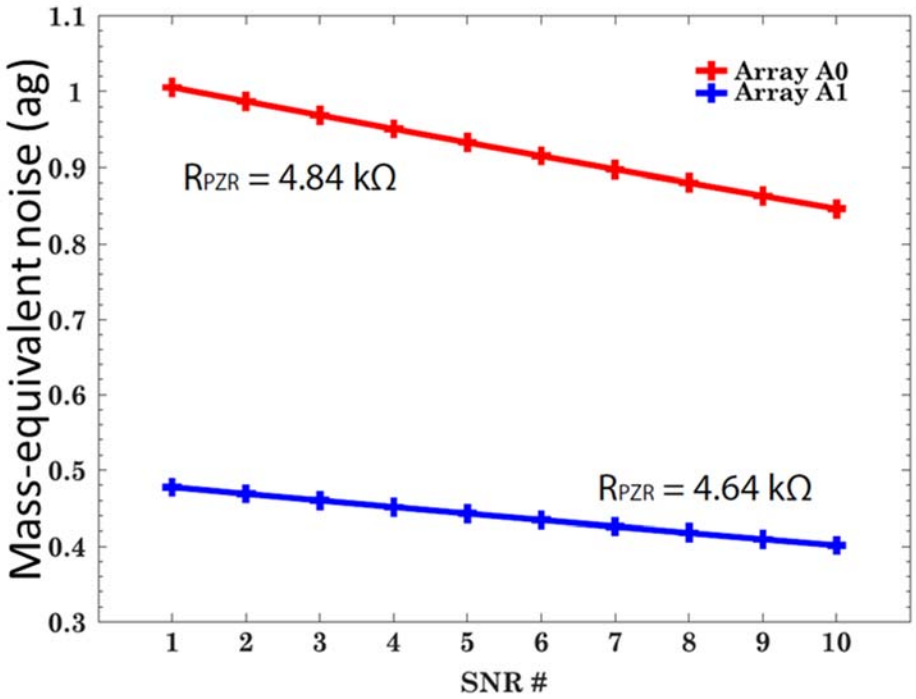

Figure S2. Estimated mass-equivalent noise of SNR # within an array A1 and array A0. The mass-equivalent noise is calculated for each SNR of arrays A0 and A1 using parameters of **Table 2** and doping profile from ion implantation simulation with a dose of $7x10^{14}$ at/cm^2 and energy of 5 keV as presented in Figure S15. As the piezoresistor length is fixed (L_{PZR} = 14 µm for A0 and L_{PZR} = 10 µm for A1), all SNRs have the same piezoresistance value while their length is varied across an array. This results in a varying mass-equivalent noise function of the SNR number in the array.

Supporting Information 3: Details for device fabrication

The device fabrication steps are detailed in the following section, and the material color chart for each illustration (**Figure S3** to **Figure S10**) is the same as the one defined in **Figure 2**. All the doping related process steps were supported by ion implantation and annealing simulations using Silvaco tools and presented in **Figure S11** to **Figure S15**.

Preparation of Bottom SOI substrate and N-type background

First, a SOI bottom wafer with the following properties was used to delineate the embedded channel: Top Silicon layer (also referred as the device layer) thickness = 400 nm (P-type doping) / BOX (Buried Oxide) layer = 1 µm / Si bulk = 725 µm / SiO_2. The SOI top layer was implanted with phosphorus dopants (N-type doping) to a dose of 10^{13} at/cm² with an energy of 140 keV (Tilt 7° Twist 27°), followed by an annealing at 950°C for 30 minutes in N2 for dopants activation. A front side epitaxy of in situ N-doped Silicon was performed (phosphorus doping $4x10^{17}$ at/cm^3 @ 950°C) to add a layer of 520 nm thick N-doped Silicon resulting in a SOI total device layer thickness of 920 nm. The front side of the wafer was then protected by a 1.5 µm thick oxide layer deposited by plasma enhanced chemical vapor deposition (PECVD), followed by laser marking to label the backside of the wafer for further identification. The front side protection PECVD oxide layer was removed by diluted HF, and a thermal oxidation was carried out in order to grow a 7 nm thick Silicon dioxide protective layer.

Embedded channel patterning

A Deep UV (DUV) photolithography and RIE etching was sequentially performed in order to define 120 nm deep alignment marks etched onto the wafer front side. The embedded channel was patterned after DUV lithography, RIE etching of both the top SiO_2 protective layer (7 nm thick)

and partial etching of the Silicon SOI layer, followed by the removal of the photoresist. We thus obtained 700nm deep and 700 nm or 1 µm wide microfluidic channels, according to the different designs. The 7 nm thick SiO_2 layer was removed by chemical etching in a 0.1 % diluted HF solution, and replaced by a 10 nm thick thermal Silicon dioxide SiO_2 as a protective screen layer for subsequent implantations.

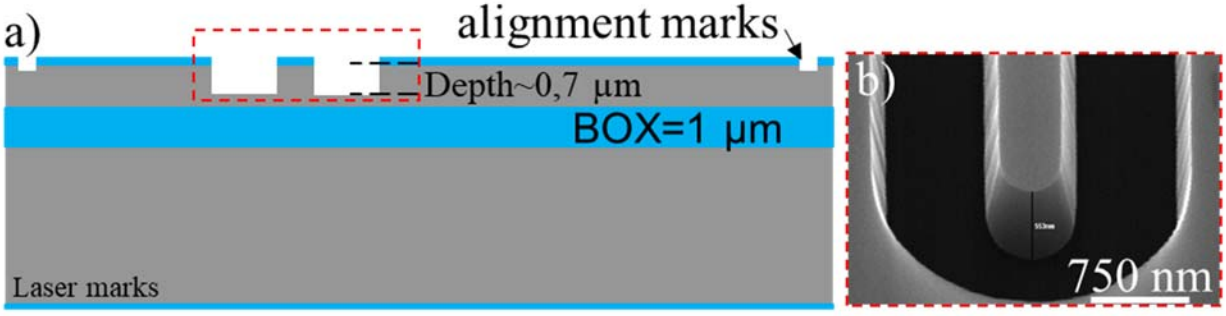

Figure S3. (a) Schematic of the device cross section after the preparation of the bottom SOI substrate, and the patterning of the embedded channel (700 nm in depth). The material color chart is the same as the one defined in **Figure 2**. (b) Illustration of a typical Scanning Electron Microscopy (SEM) tilted image of the embedded channel.

Preparation of TOP SOI substrate and fusion bonding

A top SOI wafer with the following features was used to later cover the embedded channel in the SNR resonator and to incorporate the piezoresistor therein: top Silicon device layer thickness = 220 nm (P-type doping) / BOX (Buried Oxide) layer = 2 µm / Si bulk = 725 µm. A thermal oxidation was performed at 800 °C resulting in a growth of 10 nm thick Silicon dioxide, and consuming almost 5 nm of the Silicon device layer[5]. Then, the top and bottom SOI wafers (terminated with Silicon dioxide surface) was assembled together by direct fusion bonding under vacuum (10^{-2}mbar). A subsequent high-temperature annealing was performed at 1100 °C in a steam atmosphere to increase the bond strength between the wafers. After this assembly procedure, the backside of the top SOI substrate was partially removed by coarse and fine grinding to leave a 25 µm-thick residual silicon handle, which was etched afterwards in a TMAH solution. The

exposed 2 µm thick BOX layer was fully etched in a buffered oxide solution. At this stage, a 215 nm thick silicon lid was obtained.

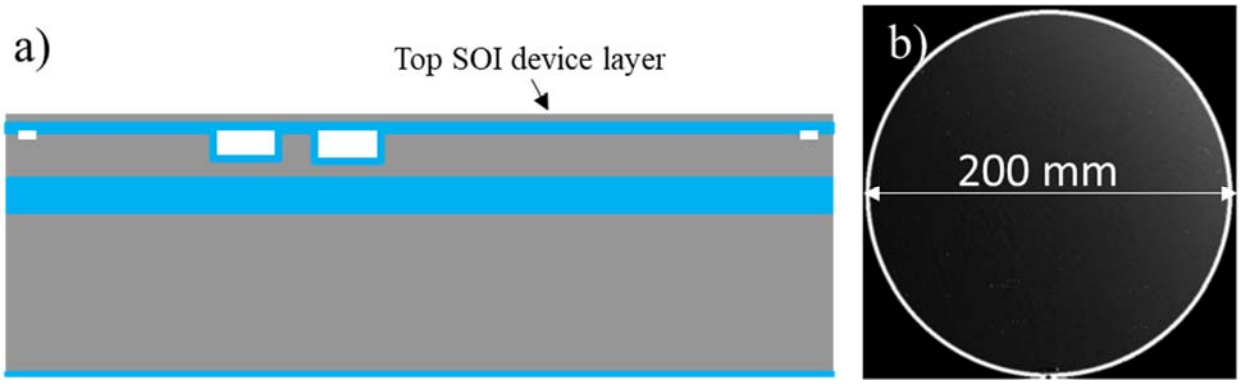

Figure S4. (a) Schematic of the device cross section after fusion bonding between top and bottom SOI wafers and top side thinning. The material color chart is the same as the one defined in **Figure 2**. (b) Scanning acoustic microscopy image of the wafer-level bonding interface, showing the absence of major bonding defect.

Implantations for background (N), traces (P++), isolation (N+), piezoresistor (p+)

A pre-implantation thermal oxidation (in O2 atmosphere) was performed at 800 °C to create a 10 nm thick SiO_2 protective layer. Phosphorus ions was implanted full sheet at 70 keV (Tilt 7° Twist 27°) with a dose of 10^{13} ions cm^{-2} to ensure a uniform isolation of the p-type piezoresistors from the substrate via the creation of PN junction.

Three sequential steps of [photolithography, implantations, stripping] were carried out in order to define (i) the P++ low-resistivity connections between the future piezoresistors and the metal pads, (ii) the surrounding N++ traces located between the P++traces, for isolation purpose, and (iii) the P+ piezoresistor. Hence, the P++ traces were defined by local implantation of boron ions at 30 keV (Tilt 7° Twist 27°) with a dose of $5x10^{15}$ ions cm^{-2}. Then, phosphorus ions were implanted at 70 keV (Tilt 7° Twist 27°) with a dose of 10^{15} ions cm^{-2} to define the N+ traces. Finally, the wafer was annealed at 1050 °C for 30 minutes under nitrogen to obtain flat doping profiles.

For the P+ piezoresistive region, boron ion implantation was performed at 5 keV (Tilt 7° Twist 27°) with a dose of $7x10^{14}$ ions cm^{-2}. Next, a spike annealing under nitrogen at 1050 °C was performed to activate the boron dopants without diffusion, resulting in a shallow piezoresistor. The implanted p-type piezoresistors are U-shaped but mostly parallel to the <110> direction to maximize the gauge factor. The junction depth for the piezoresistive area is estimated to be around 0.1 μm which is less than the top silicon device layer remaining thickness (~210 nm after the two thermal oxidation steps), ensuring electrical isolation from the fluid which could be conductive. In addition, the doping levels in the piezoresistor and the surrounding n-well are sufficiently high to prevent full depletion on either side when the junction is reverse-biased.

TEOS passivation and metal pads/traces

Previous studies have shown that contamination by sodium from the borofloat glass wafer occurs during anodic bonding[6]. In order to isolate the piezoresistor and background areas from potential contamination, a 500 nm thick TEOS (Tetra-Ethyl-Ortho-Silicate) oxide layer was deposited by PECVD at 400 °C onto the wafer front side. A chemical-mechanical polishing (CMP) was performed on the TEOS layer to reduce the surface roughness and enhance the bond strength with the glass wafer. This resulted in the removal of 100nm of the TEOS layer. The TEOS oxide was patterned to delineate the contact pad areas prior to metallization. Then a 650 nm thick AlSi layer was deposited by sputtering and chemically etched (especially with “freckle etch” formulated to remove any residual silicon nodules from the AlSi layer) to pattern aluminum pads and traces. These last ones cover both the boron-doped P++ traces connecting piezoresistors with bonding pads and the N+ isolation traces in order to further decrease the electrical resistance. Across the different devices and wafers, we experimentally measured piezoresistances values of 5 to 6 kΩ,

which are on the same order of magnitude as estimated values given by the optimization: 4.84 kΩ and 4.64 kΩ for A0 and A1 arrays respectively (**Figure S2**).

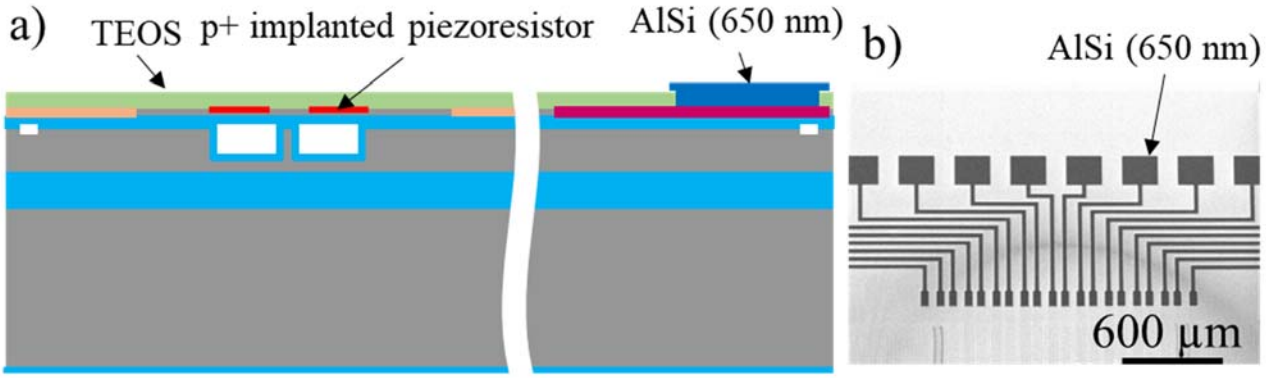

Figure S5. (a) Schematic of the device cross section after the sequences of implantations for definition of the background, traces, isolation, and piezoresistor, the coating with a TEOS layer, and the pattering of metal pads (AlSi 650 nm). The material color chart is the same as the one defined in **Figure 2**. (b) Illustration of a typical Scanning Electron Microscopy image of the metal pads and traces for addressing the readout of each cantilever of the array

SNR patterning

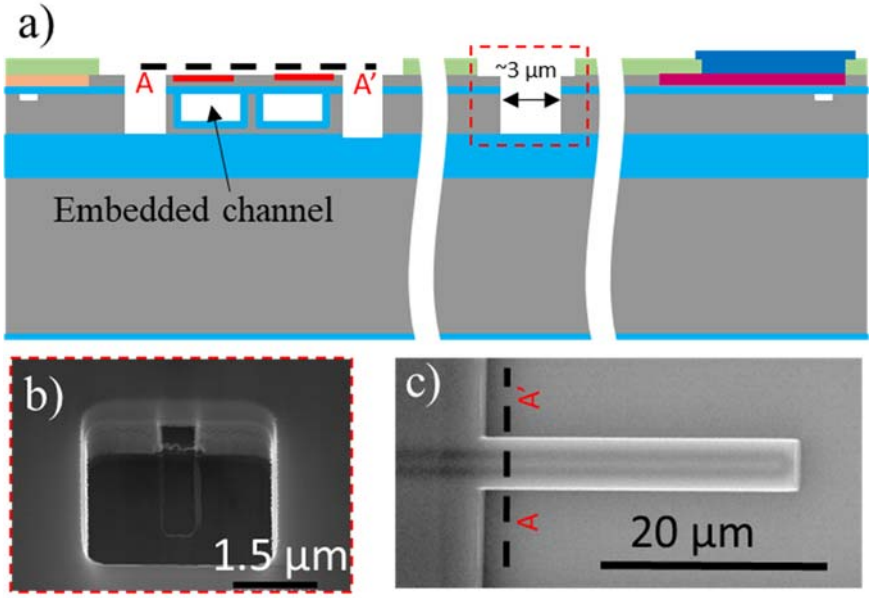

Figure S6. (a) Schematic of the device cross section after the sequences for patterning the front-side TEOS oxide, the trenches surrounding a cantilever and the inlet ports to the embedded channel. The material color chart is the same as the one defined in **Figure 2**. (b) Close view Scanning Electron Microscopy image of the access port towards the embedded channel. (c) Scanning Electron Microscopy image of a SNR.

Next, the TEOS oxide was patterned and removed from the surface above the region for each cantilever to minimize bending due to the thermal expansion mismatch between the different layers. Next, the cantilever was defined by DUV lithography followed by RIE etching. A 10 µm wide U-shaped trench was patterned through the top 210 nm thick silicon layer, the 20 nm thick intermediate SiO_2 layer (used for fusion bonding) and the 920 nm silicon layer of the bottom SOI. At the same time, squares shaped access ports are etched to define inlet ports towards the embedded channel. SEM images of the SNR and access port towards the embedded channel are both shown on **Figure S6**.

Preparation of borosilicate glass and anodic bonding

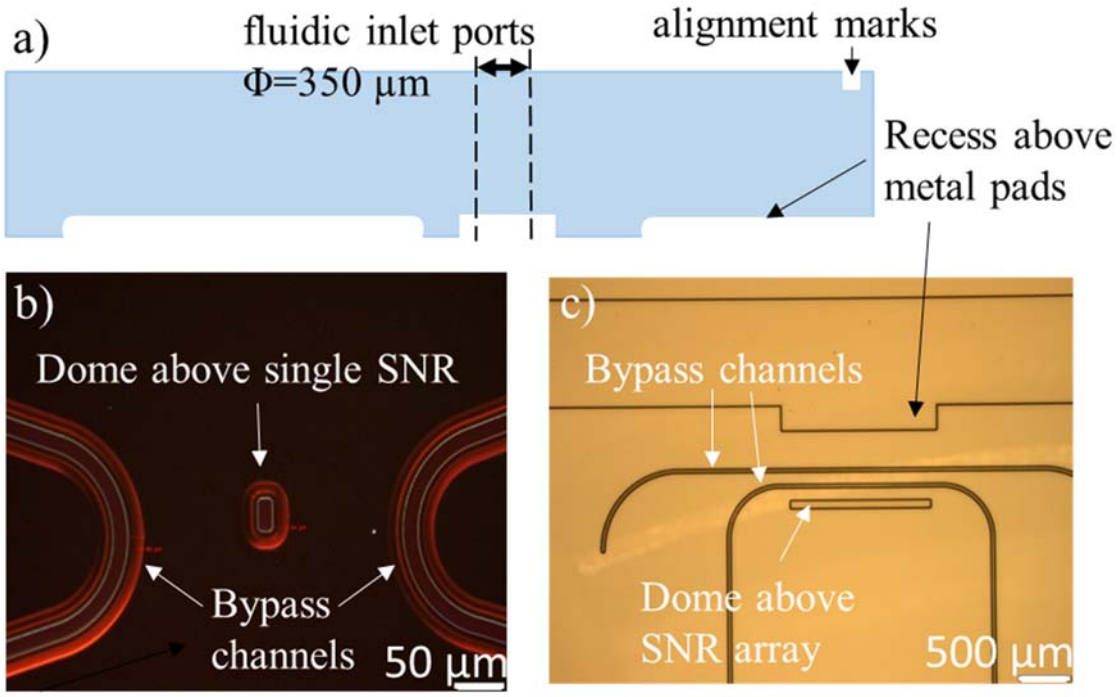

Figure S7. (a) Schematic of the glass part cross section after the chemical etching steps (-10 µm in depth) to define the bypass channels, the dome above SNR(s) and the recess above metal pads. The material color chart is the same as the one defined in **Figure 2**. (b) Dark field microscopy image of the glass wafer for a single SNR design. (c) Bright field microscopy image of the glass wafer for a SNR array design.

A 500-µm thick borofloat 33 glass substrate was used as a lid wafer incorporating fluidic ports, bypass channels and a dome above SNRs and metal pads. First, a standard SC1 cleaning followed by piranha was performed to clean the wafer. A 1µm thick amorphous silicon layer was deposited to protect both sides of the wafer. The backside was patterned to define alignment marks etched by RIE through the amorphous silicon and down to 500 nm deep into the glass wafer. Then the bypass channels for fluid delivery to the SNRs was patterned onto the front side by photolithography and chemical etching down to 10 µm in depth, resulting in 10 µm lateral etching. At the same step, the dome cavity above the SNR(s) was etched, as well as some recessed areas above the future metal pads. Finally, the amorphous silicon layer was removed in a 1 % diluted HF solution, followed by TMAH immersion at 90 °C for 30 seconds. The glass wafers were then

ultrasonically drilled (Bullen Ultrasonics Inc.) through the entire thickness to define the inlet/outlet fluidic ports communicating with the bypass channels.

After HF 1% and SC2 cleaning for surface particles removal, the glass wafer was aligned and brought into contact with the SOI wafer hosting SNRs, followed by anodic bonding under primary vacuum, at 400 °C for 15 minutes with 3 kN, -700 V, applied pressure and voltage respectively. The glass surface has been protected with UV tape, and the SOI backside was grinded to create a 200 µm thick silicon bulk layer. Next, 5 µm deep trenches were defined on the backside of the bottom SOI substrate by photolithography and RIE etching on the periphery of each chip in order to surround the future cavity with the getter. The purpose of these trenches is to retain excess molten gold resulting from the final eutectic bonding step in order to prevent it from penetrating into the getter cavity. A backside photolithography was carried out, followed by deep RIE etching to remove both the silicon and the buried oxide layer (BOX) from the bottom SOI substrate to release each cantilever. Etching time was adjusted to reduce etching impact on the SNR bottom lid.

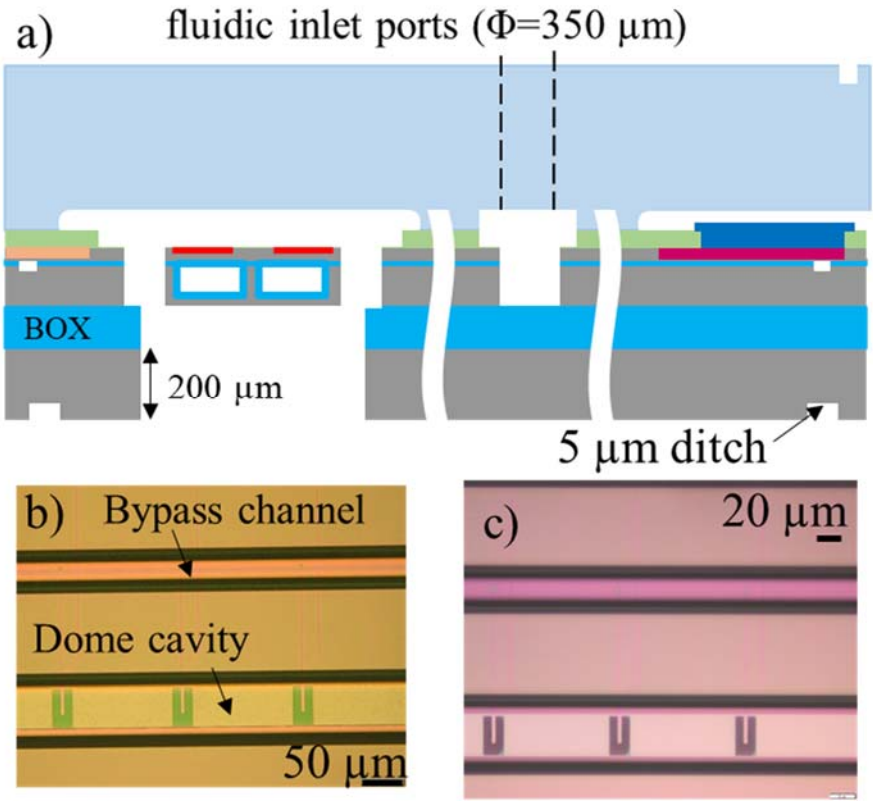

Figure S8. (a) Schematic of the device cross section after the glass wafer anodic bonding, the backside grinding of the bottom SOI wafer (thickness thinned down to 200 µm) and the SNR cantilever releasing (RIE etching of bottom bulk Si + BOX layer). The material color chart is the same as the one defined in **Figure 2**. (b) Bright field microscopy image for a SNR array after the anodic bonding with the Glass. (c) Bright field microscopy image for a SNR array after the backside releasing of each cantilever.

Preparation of wafer for hosting a getter

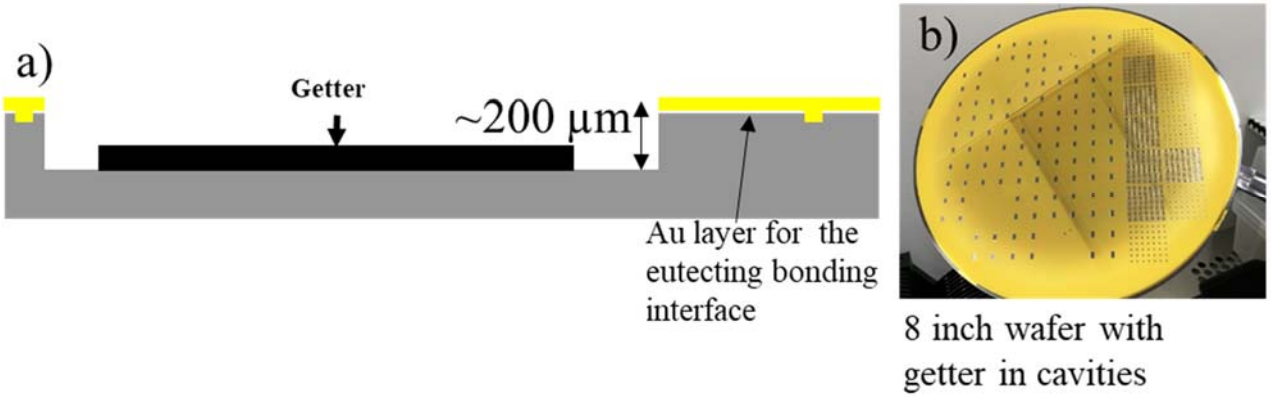

Figure S9. (a) Schematic of the bottom Silicon wafer part cross section after the coating of Au layer for eutectic sealing, etching of a 200 µm deep cavity and local deposition of a getter material into the recess floor. The material color chart is the same as the one defined in **Figure 2**. (b) Optical picture of the resulting wafer.

Double side polished Si wafers were processed in order to define a cavity for the on-chip getter material to ensure stability of the SNR low pressure micro-environment over extended time. First, a Cr/Au bilayer was deposited and patterned by photolithography and chemical etching. The exposed silicon was anisotropically etched by ICP to define a 200-µm deep cavity. A getter material was deposited through a shadow mask into the cavity bottom floor (SAES getter).

Lastly, eutectic bonding between the SOI wafer and the substrate hosting the getter was performed at 430 °C under 30 kN in order to place each cantilever in a vacuum sealed cavity.

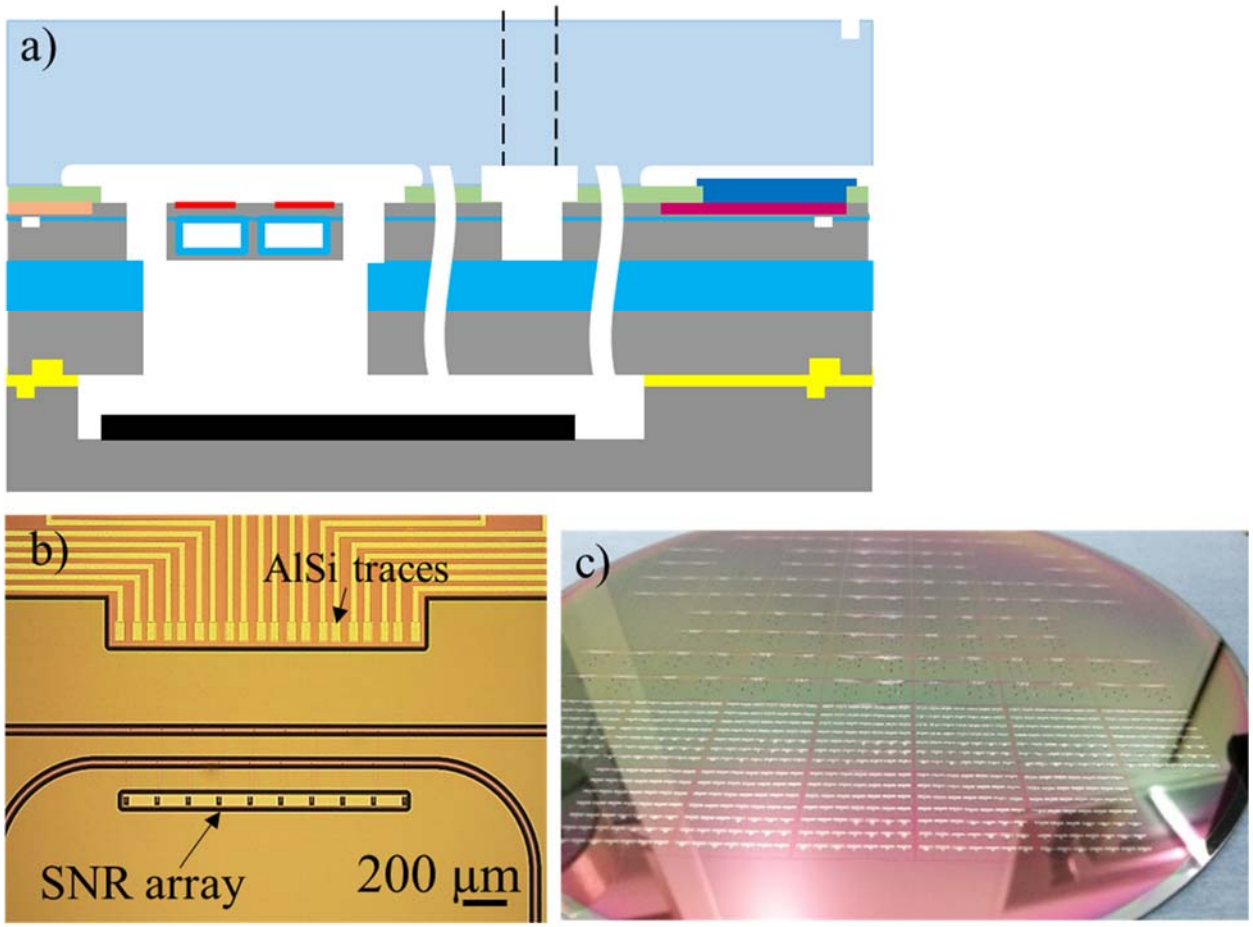

Figure S10. (a) Schematic of the device cross section after the final eutectic bonding in vacuum with the wafer housing the getter material. The material color chart is the same as the one defined in **Figure 2**. (b) Bright field microscopy image for a device hosting an array of SNRs at the final stage of fabrication. (c) Picture of the resulting 8-inch wafer and devices.

Supporting Information 4: Simulations on ion implantation and annealing for all the doping steps

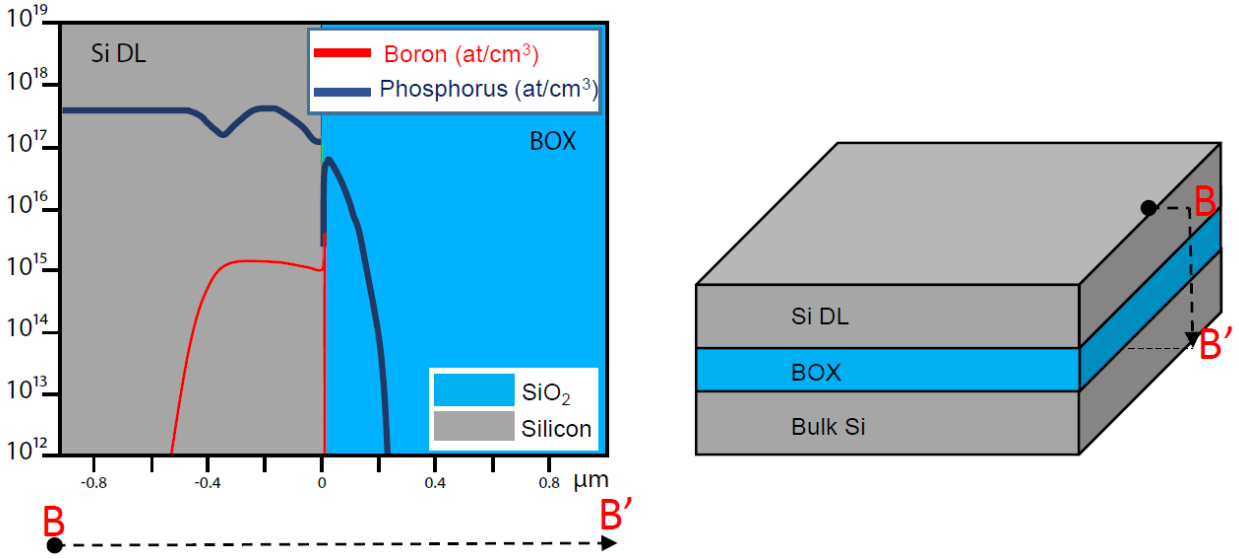

Figure S11. Simulated dopant concentration profiles in the bottom SOI after full sheet implantation of phosphorous 10^{13} at/cm^2 at 140 keV, annealing at 950 °C for 30 minutes in N2, and 520 nm growth epitaxy of silicon with in-situ phosphorous dopants at a concentration of 4x10^{17} at/cm^3. Here *Si DL* refers to the device layer of the bottom SOI wafer, and BOX is the buried xxide layer insulating the device layer with the bulk silicon layer. The simulated profile is almost flat through the device layer with phosphorus dopants concentration ranging from 2 to 4x10^{17} at/cm^3.

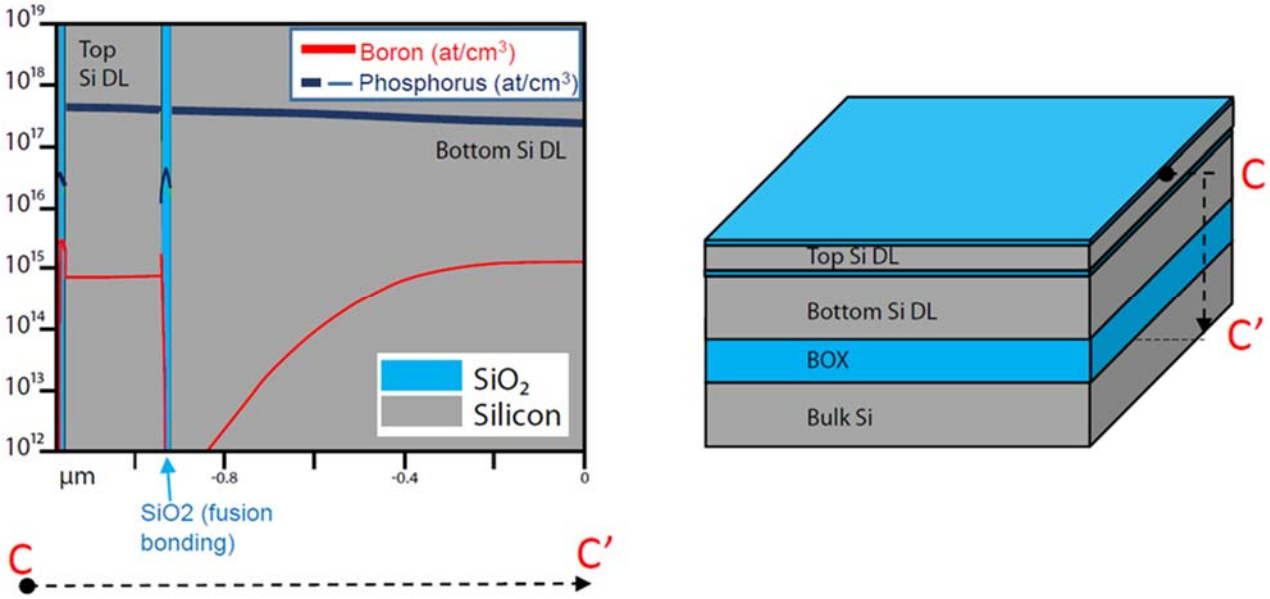

Figure S12. Simulated dopant concentration profiles (from Silvaco Athena tool) across the bottom and top SOI wafers after their fusion bonding (using 10 nm/10 nm thick SiO_2 interfaces), thermal oxidation to grow SiO_2 screen layer (~10 nm @ 800 °C), phosphorous implantation (10^{13} at/ cm^2 at 70 keV) and dopants activation (annealing at 1050 °C for 30 minutes in N2). This results in an almost flat N background doping across the full stack (between 2.5 to 4.5x10^{17} at/ cm^3). Here *Top*

Si DL refers to the device layer of the top SOI wafer, and *Bottom Si DL* the device layer of the bottom SOI wafer.

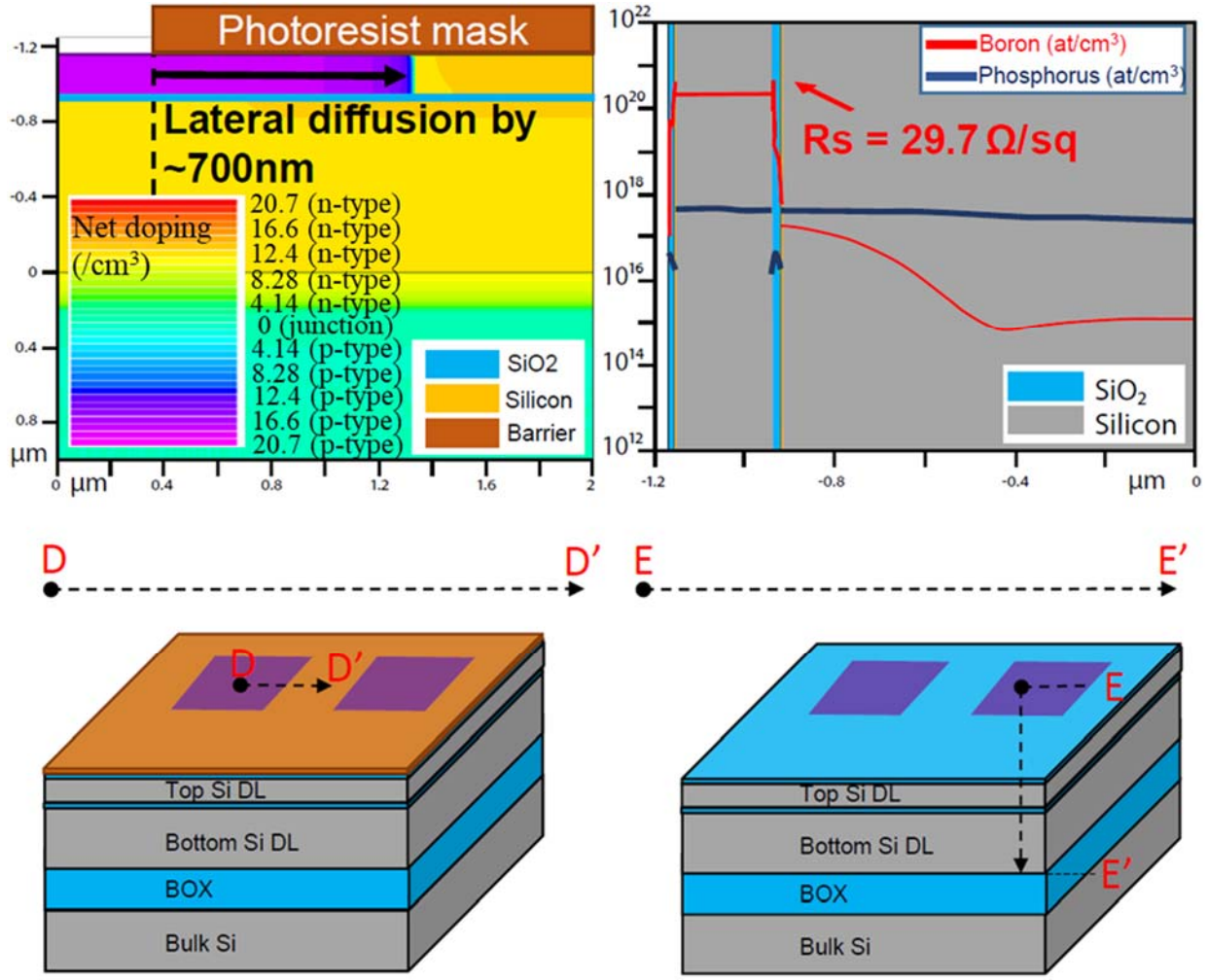

Figure S13. Simulated dopant concentration profiles (from Silvaco Athena tool) for the P++ trace doping achieved by implantation of boron dopants ($5x10^{15}$ at/cm^2 at 30 keV) followed by annealing at 1050 °C for 30 minutes in N_2. {left} Simulated 2D boron concentration profile across the full stack after annealing. The lateral Boron diffusion sets the minimal gap between the trace and isolation doping patterns. The color scale on the plot represents net doping levels in *at/cm*^{3}: red to green colors are for n-type doping from high to low levels, green to purple color are for p-type doping. {right} The p++ trace doping is about $2x10^{20}$ at/cm^3 with a flat profile across the top SOI layer, leading to a sheet resistance of 29.7 ohm/square. The SiO_2 bonding interface (20 nm) between both SOI wafers limits the diffusion inside the bottom SOI silicon layer.

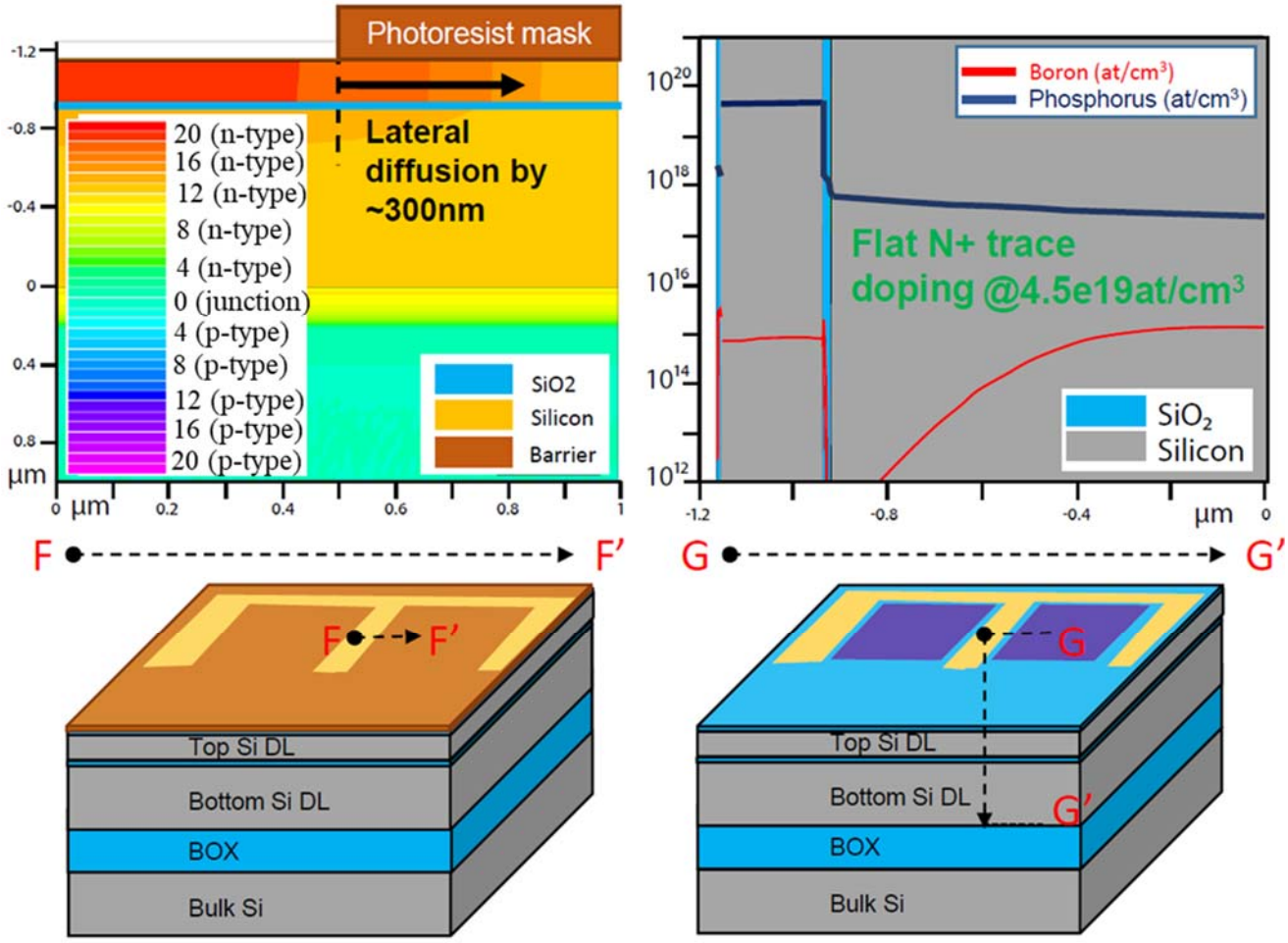

Figure S14. Simulated dopant concentration profiles (from Silvaco Athena tool) for the N+ isolation doping achieved by implantation of phosphorus dopants (10^{15} at/cm^2 at 70 keV) followed by annealing at 1050 °C for 30 minutes in N_2. {left} Simulated 2D phosphorous concentration profile across the full stack after annealing. The lateral phosphorous diffusion adds to the boron diffusion to set the minimal gap between the trace and isolation doping patterns. As the phosphorous diffuses less than boron species in silicon, the lateral diffusion is reduced for the same annealing conditions. The color chart corresponds to the net doping (/cm^3). {right} The n+ isolation doping is about 4,5x10^{19} at/cm^3 with a flat profile across the top SOI layer.

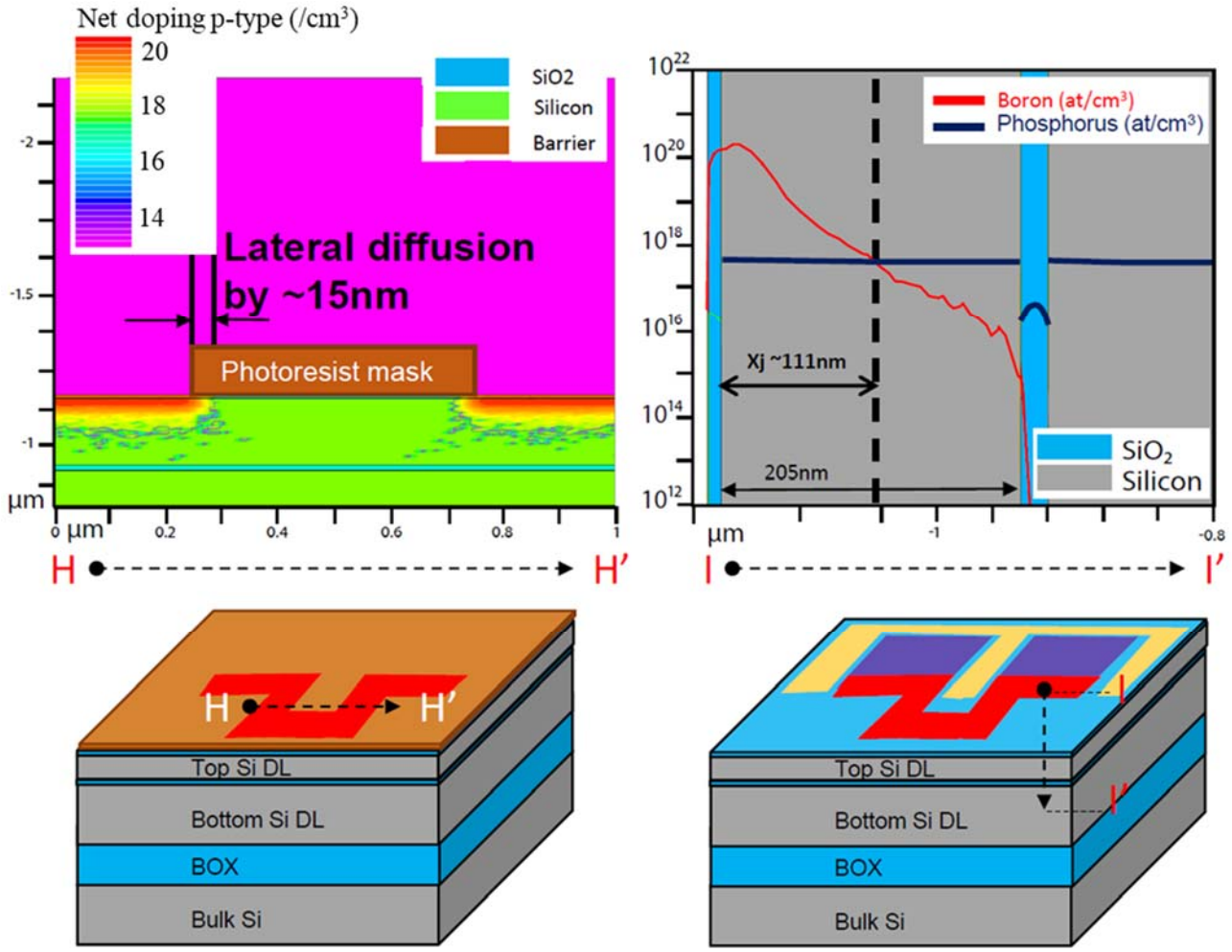

Figure S15. Simulated dopant concentration profiles (from Silvaco Athena tool) for the P+ Piezo doping achieved by implantation of boron dopants ($7x10^{14}$ at/cm^2 at 5 keV) followed by a spike annealing at 1050 °C under N_2. The color scale represents the net p-type doping from highest (red) to lowest (purple) concentrations. {left} Simulated 2D boron concentration profile across the top lid layer, bonding interface and top of the bottom Si layer after spike annealing. The spike anneal even at high temperature prevents the boron to diffuse and hence allow a good control of the piezo doping profile. {right} The P+ piezo doping leads to a junction depth of ~111 nm.

Supporting Information 5: Readout circuitry

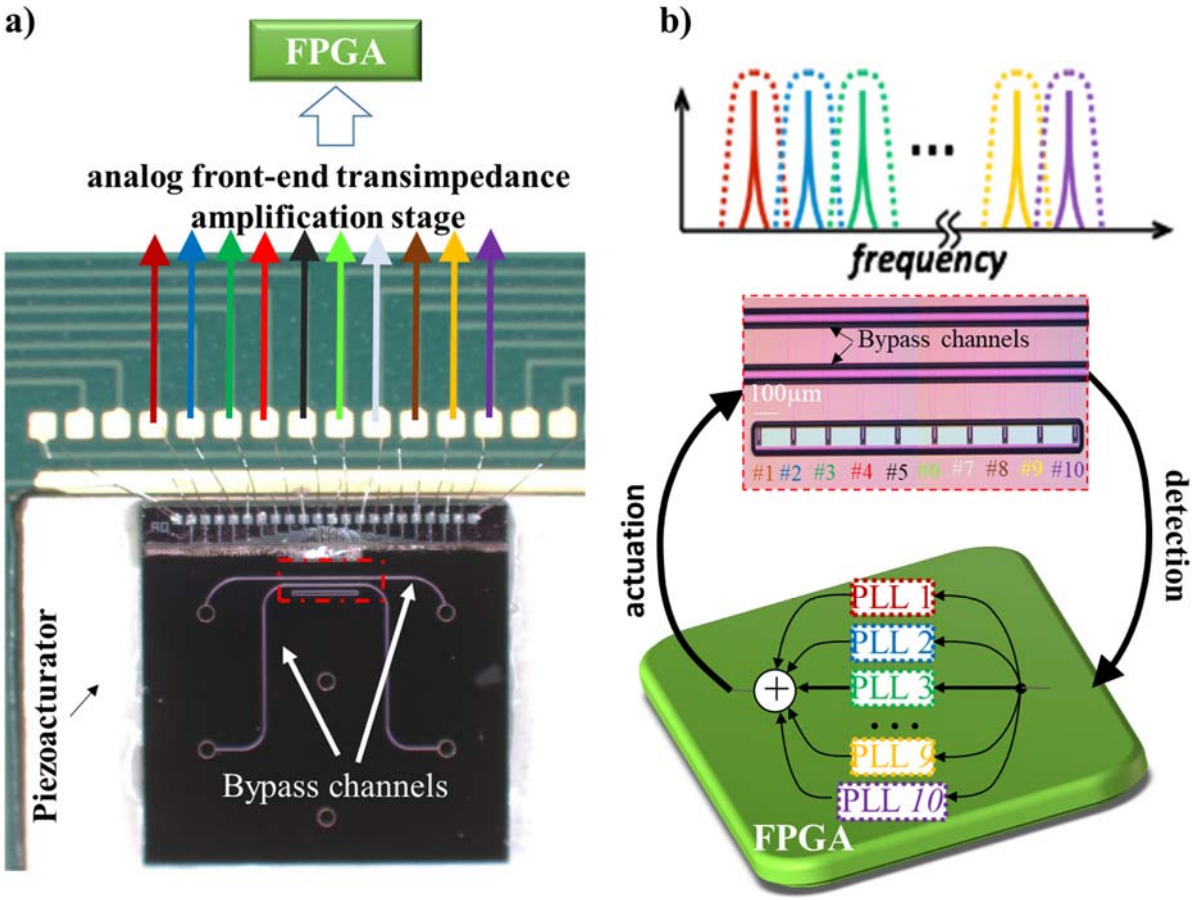

Figure S16. a) The SNR is bonded onto a Printed Circuit Board (PCB) platform hosting a piezoceramic actuator. Each metal pad connected to the piezoresistor of each resonator is wire bonded onto its corresponding pad onto the PCB. One lead of the piezoresistors are connected together at a pad, where a piezoresistor bias voltage is applied. The other lead is individually bonded to a pad. The signal at each piezoresistor is first amplified through a transimpedance amplifier. Then the neighboring piezoresistor signals are amplified together by a differential amplifier with a high common mode rejection ratio to suppress the common mode interference noise. All output signals are then summed together to create the total deflection signal which contains the N frequency components. This total analog signal is then converted to a digital signal through an analog to digital convertor and directed to an array of N phase-locked loops (PLLs) implemented in a field-programmable gate array (FPGA). (b) Each PLL locks to the unique resonant frequency of a single SNR cantilever, similarly to what has been previously developed[7]. Therefore, there is a one-to-one pairing between cantilevers and PLLs, and the signal from each resonator does not require a pass-band filter. Each PLL locks to the assigned cantilever's resonant frequency and demodulated the deflection signal. The numerically controlled oscillators in the PLLs generate a sinusoidal drive signal at that frequency. The drive signals from each PLL are summed, amplified and used to drive a single piezoceramic actuator positioned directly underneath the chip, which completes the feedback loop. Each PLL is configured such that it will track its cantilever's resonant frequency with a measurement bandwidth of typically 100 to 1,000 Hz.

Supporting Information 6: Calculation of limit of mass detection from experimental data

To determine the detection limit in terms of buoyant mass, we measured the stability of the resonance frequency baseline for our SNR devices for 15 minutes as they were locked in the PLL mode when the resonators did not contain liquid. For these noise experiments, we set the cascaded integrator–comb filter to $CIC_{rate} = 2{,}500$ and the data decimation to $\mathrm{decim} = 4$.[7] Given that the data-rate of our FPGA is set by its clock $f_{FPGA} = 100\ MHz$, the sampling rate was then:

$$f_s = \frac{f_{FPGA}}{CIC\ x\ decim} = 10{,}000\ Hz \qquad \text{Equation 6}$$

With the measurement bandwidth set to $1{,}000\ Hz$, we recorded the baseline resonance frequency over time $f_r(t)$ with sampling rate f_s leading to a total of $N_{total} \cong 900 \times f_s$ data points for every experiment. We then averaged $f_r(t)$ over different time intervals τ (or average gate time) and calculated the root mean square of the difference between the means of $f_r(t)$ for subsequent time intervals. We thus computed the Allan deviation:

$$\sigma_A(\tau) = \sqrt{\frac{1}{2(N-1)} \sum_{k=2}^{N} \left(\frac{\bar{f}_k - \bar{f}_{k-1}}{f_o} \right)^2} \qquad \text{Equation 7}$$

In

$\sigma A(\tau)=12(N-1)k=2Nfk-fk-1fo2$

Equation 7, we calculated the averaging (gate) time τ based on the number N of possible truncations (halvings) of the data:

$$\tau = (N_{total}/f_s)/2^N \qquad \text{Equation 8}$$

Note that the Allan Deviation $\sigma_A(\tau)$ represents a normalized change of frequency $\Delta f/f$. As such we converted it to absolute mass units in attograms by using the effective mass of the cantilever using the relationship[8]:

$$\Delta m = 2\, m_{eff} \frac{\Delta f}{f} \qquad \text{Equation 9}$$

Note that the effective mass m_{eff} is also extracted using Equation 9, since the ratio $\frac{\Delta f}{\Delta m} = R_m$ is the known mass sensitivity of the device in use, and $f = f_r$ is the median of the resonant frequency. We then got that the effective mass is:

$$m_{eff} = \frac{f_r}{2R_m} \qquad \text{Equation 10}$$

The limit of detection is then:

$$\Delta m = \frac{f_r}{R_m}\sigma_A(\tau) \qquad \text{Equation 11}$$

The calibration of SNR devices is performed by measuring the resonance frequency shifts caused by the flow of size-calibrated (CV < 8%) gold nanoparticles through the cantilever. We then divided the mean resonance frequency shift by the known nanoparticles buoyant mass to estimate the mass sensitivity of a given device:

$$R_m = \frac{\Delta f_{mean}}{m_B} \qquad \text{Equation 12}$$

We calculated the theoretical limit of detection using a prior analysis of liquid-based mass detection with suspended microchannel resonators[2] where the symbols are the same as in Supplementary Information 2:

$$\sigma_{A,non}^{th}(\tau) = \frac{1}{5.46L}\sqrt{\frac{k_B\,T}{\tau\,k\,f_o}} \qquad \text{Equation 13}$$

Equation 13 is derived from Equation 1 and represents a theoretical minimum for the mass-equivalent noise for a cantilever that is driven at the onset of non-linearity. This theoretical minimum represents the noise induced due to thermal noise and does not depend on the quality factor of the resonator.

Notably, in the case of simultaneously actuated cantilevers, the limit $\sigma_{A,non}^{th}(\tau)$ imposed by Equation 13 is different. For simplicity, we show only the limit for the cantilever with the highest frequency with different resonance frequencies f_o and lower length L. Given the variation of f_o and L within the arrays A0 and A1 (Table 2), the limit $\sigma_{A,non}^{th}(\tau)$ has a relative variation of less than 0.2%. We assumed the detection limit from a single cantilever was representative for all the cantilevers of the array.

Supporting Information 7: Experimental results

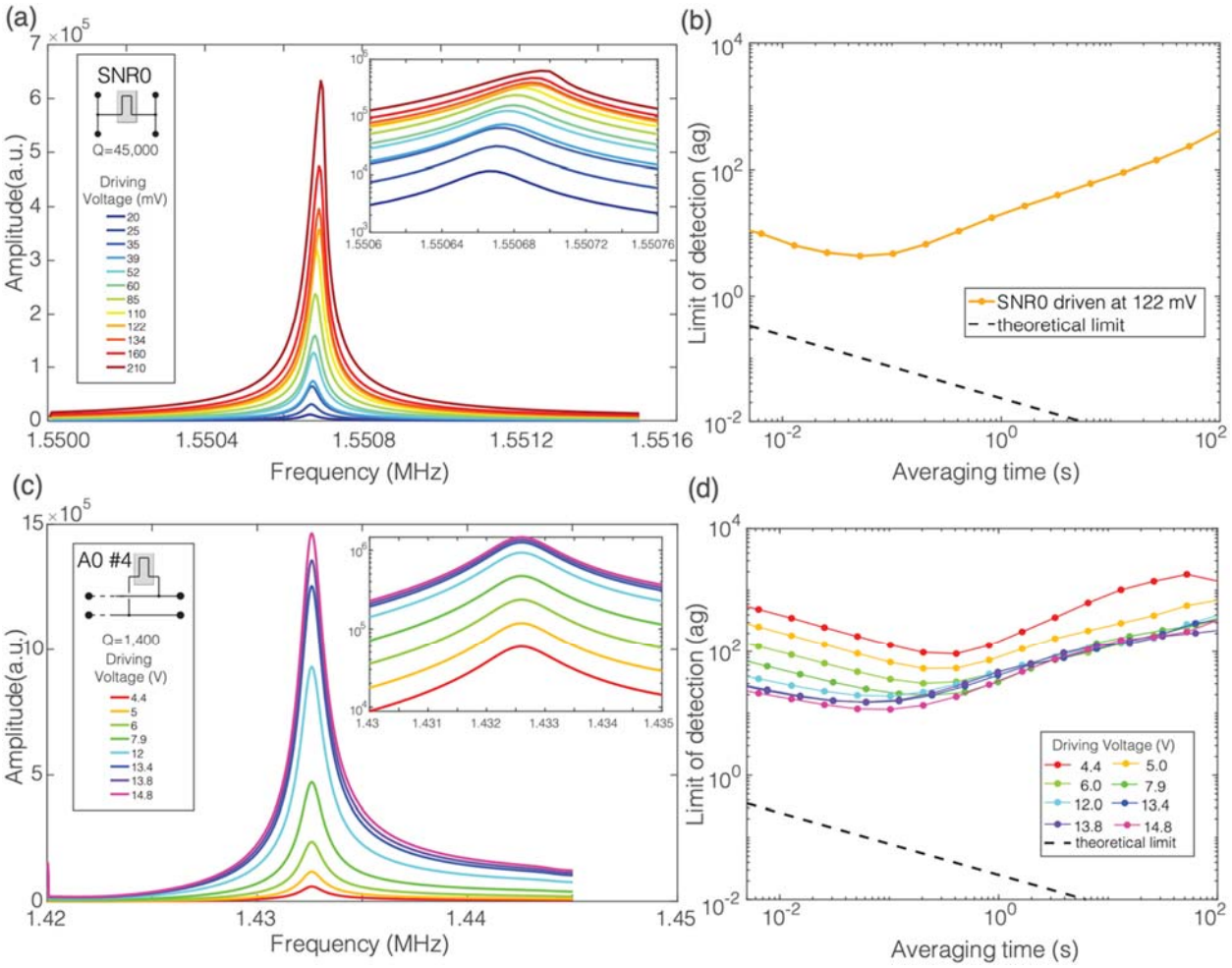

Figure S17. Frequency stability analysis of a single and array SNR as a function of driving voltage of the piezoceramic plate actuating the cantilever. (a) Frequency transmission responses of a single SNR0 resonator with a quality factor Q of 45,000 for different driving voltages (colored curves). The inset shows the response near the resonant frequency and shows characteristic bending of curves when approaching the non-linear regime. (b) Buoyant mass limit of detection obtained from the Allan deviation for SNR0 driven at 122 mV. (c) Frequency transmission responses of a SNR resonator #4 from array A0 with a quality factor Q of 1,400 for different driving voltages (colored curves). The inset shows the response near the resonant frequency. (d) Buoyant mass limit of detection obtained from the Allan deviation for SNR resonator #4 from array A0 at the driving voltages shown with the same colors as in (c). Measurement bandwidth is 1 kHz for (b,d). All measurements of (a-d) are performed without liquid in the resonators.

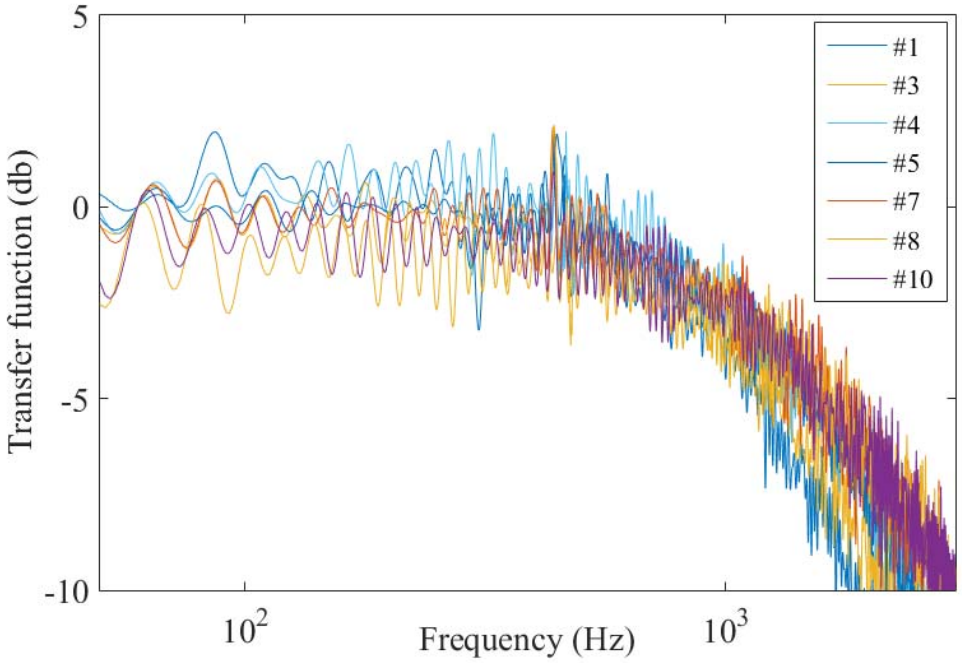

Figure S18. Measured PLL transfer functions for different PLL controllers implemented to operate cantilevers simultaneously in closed-loop within a parallel SNR A1 array. The numbers correspond to the measured PLL transfer functions for each cantilever of the device used for the experiment in figure 3b. According to the method in[7], we show that each PLL-resonator loop has a control bandwidth around 1,000 Hz.

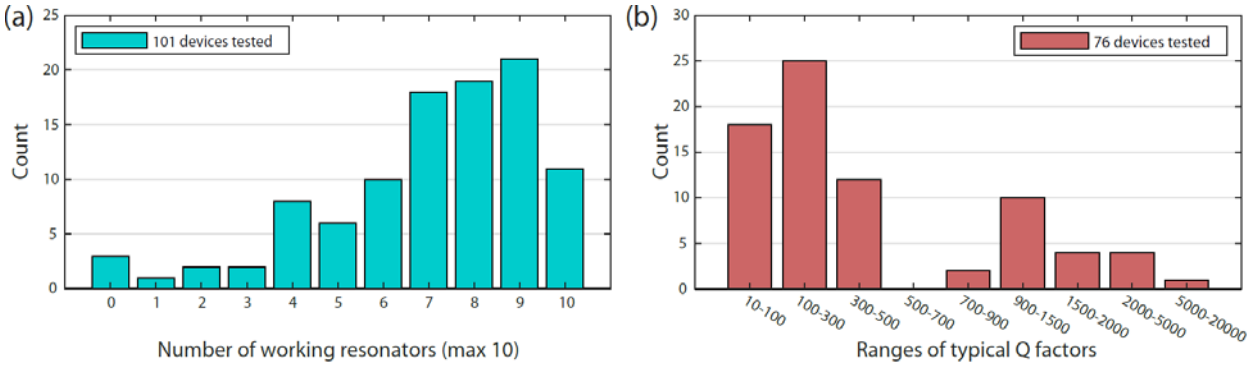

Figure S19. Statistics of tested parallel SNR arrays. (a) A total of 101 parallel SNR array devices (A0 and A1) were tested as the embedded channels were still empty (without any fluid loaded in the chip) after being glued onto the PCB hosting the piezoceramic actuator. Typically, only 7 – 9 resonators out of the 10 that are built have a resonant frequency which can be retrieved in open-loop by the sensing board. Only a few (> 10) of the tested parallel SNR array dies had all 10 resonators being functional. (b) Overall, within the same array, the typical quality factors of embedded resonators were equivalent to one another and out of 76 tested chips, a significant number of devices (> 40) showed a quality factor Q < 300: the vacuum sealing of the chamber containing the resonators may not be as efficient as single-resonator SNRs considering that the

distance with the closest embedded channel is smaller for the case of the parallel SNR array layout and the anodic bonding with the glass may not be optimized. We observed empirically that only parallel SNR array chips containing resonators with quality factors > 300 could be effectively locked by the PLL.

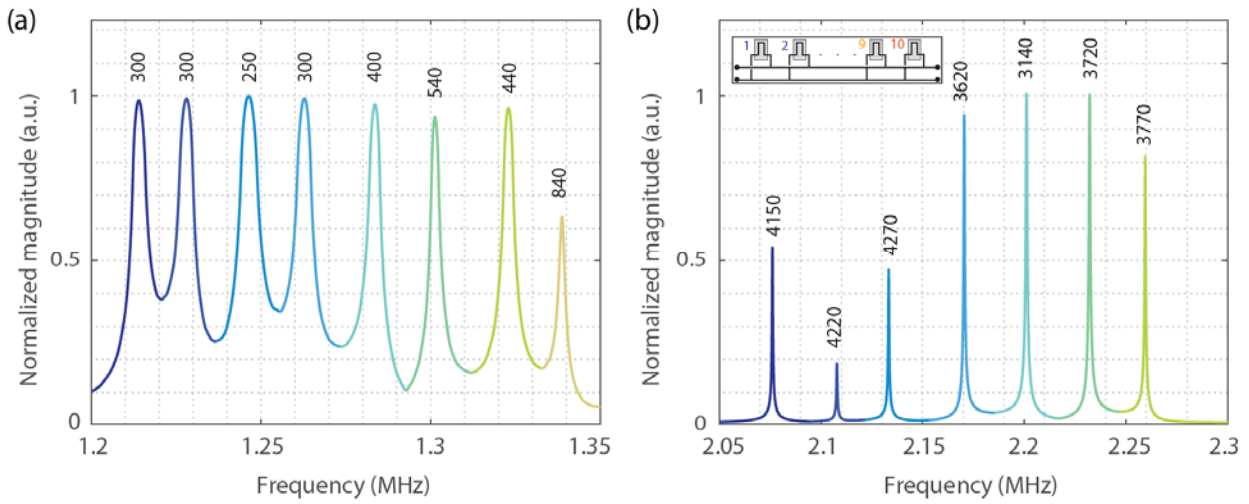

Figure S20. Frequency transmission responses of a low-Q 8-resonators parallel SNR array of type A0 (a) and high-Q 7 parallel SNR array of type A1 (b). Crosstalk occurs in the low-Q device and the noise of each resonator in the array will be affected by its adjacent SNRs. We anticipate further improvements to the sensing circuitry can include a more selective band-pass filter per each resonance frequency. The resonance peaks in the high-Q device are clearly more separated from one another: parallel SNR array devices of this kind can reach a resolution of the order of tens of attograms and the crosstalk is negligible.

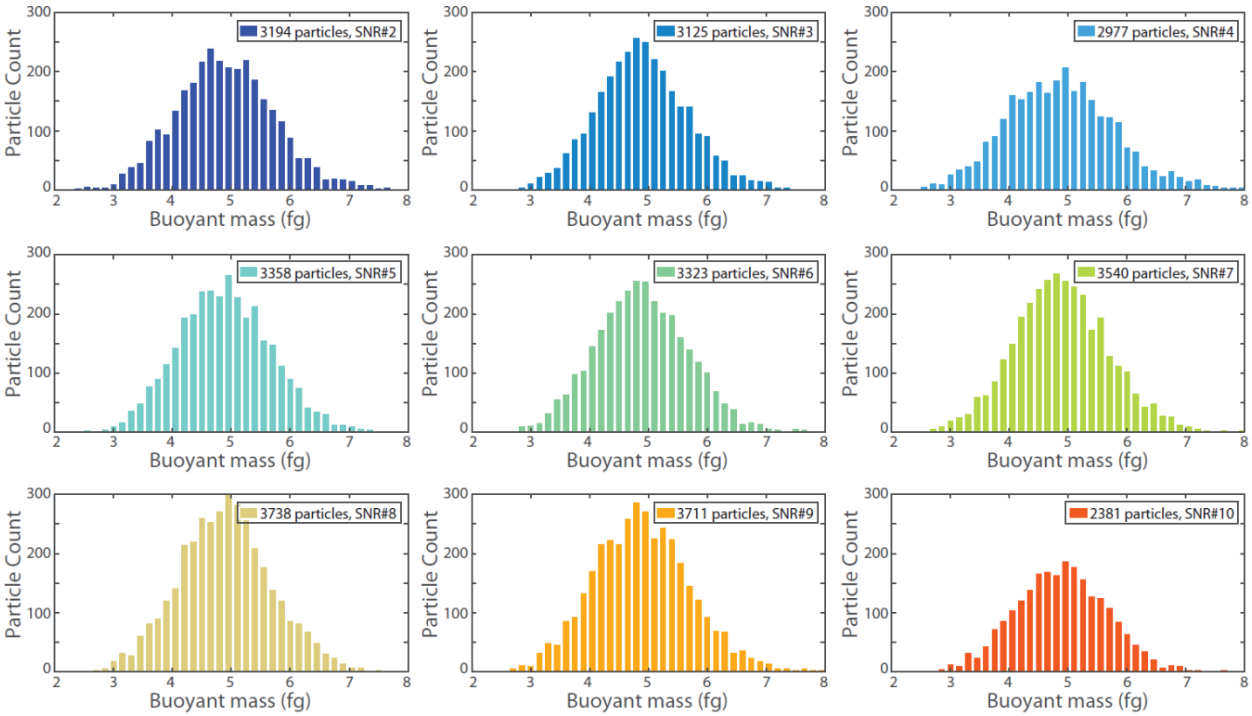

Figure S21. Buoyant mass measurements of 80 nm-diameter gold nanoparticles from 9 resonators in a parallel SNR array of type A0. Plots and data from **Figure 4a, c** are merged from these 9 sets. Throughput, CV and average buoyant mass are the same throughout the different 9 SNRs in the array.

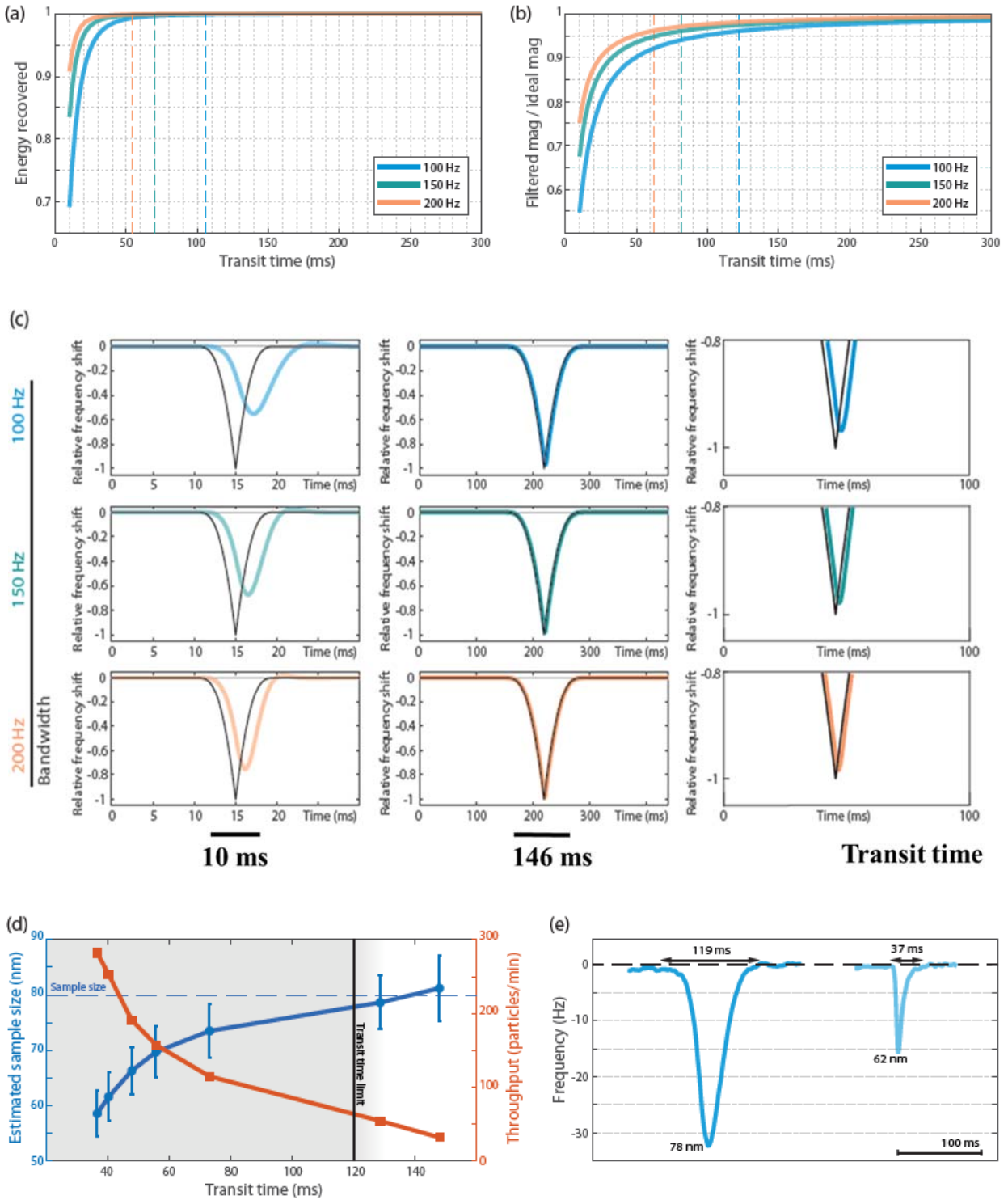

Figure S22. Transit time limit analysis. (a, b) Modeling of the distortion of the resonance frequency shift peak caused by the second order Butterworth low-pass filter in the PLL[7,9]. Energy recovery rate and peak magnitude of the filtered peak with respect to the ideal shape versus transit time of particles in the embedded channel. Parametric sweep of three typical measurement bandwidths. The dashed lines correspond to the limits above which the recovered energy of the

distorted peak with respect to the ideal one is >99.9 % (a) and the distorted peak magnitude is > 96 % the ideal peak (b). These two constraints correspond to a dimensionless transit time $\tau_{transit}$ x BW of 10 and 12 respectively for b) and a). Using similar criterion as in a previous work[9], the latter more conservative factor was chosen to set either the measurement bandwidth or the transit time in the measurements performed for this work. (c) Analytical model of ideal (black lines) versus distorted (colored lines) peak shapes with different measurement bandwidths and transit times. (d) Estimated sample size of 80 nm-diameter gold nanoparticles as measured through a SNR0 with a dimensionless transit time $\tau_{transit}$ x BW of 12. The distortion of the resonance frequency shift peak causes an underestimation of the sample size if the transit time is below the limit imposed by the measurement bandwidth, 100 Hz in this case (grey area). In particular, the results of this analysis show that for a transit time set at 61% of the limit, the mean size estimation is only affected by an error of 8%. (e) Resonance frequency shift peaks of two 80 nm-diameter gold nanoparticles passing through a SNR0 resonator embedded channel at different flow rates, while the measurement bandwidth is set to 100 Hz. For the measured frequency shift peak corresponding to a nanoparticle transit time of 119ms across the SNR, the flow rate of the nanoparticle is set to ensure that the dimensionless transit time $\tau_{transit}$ x BW is very close to the threshold 12, and 99.9% of the signal energy being recovered. For the measured frequency shift peak corresponding to a nanoparticle transit time of 37 ms, the flow rate is higher, the dimensionless transit time $\tau_{transit}$ x BW is lower than 12, and our standard criterion to require that the peak shape be fully resolved (i.e., >99.9% energy recovery) is not met. The frequency shift response is distorted, leading to an underestimation of the nanoparticle buoyant mass and diameter (here 62nm instead of 80nm).

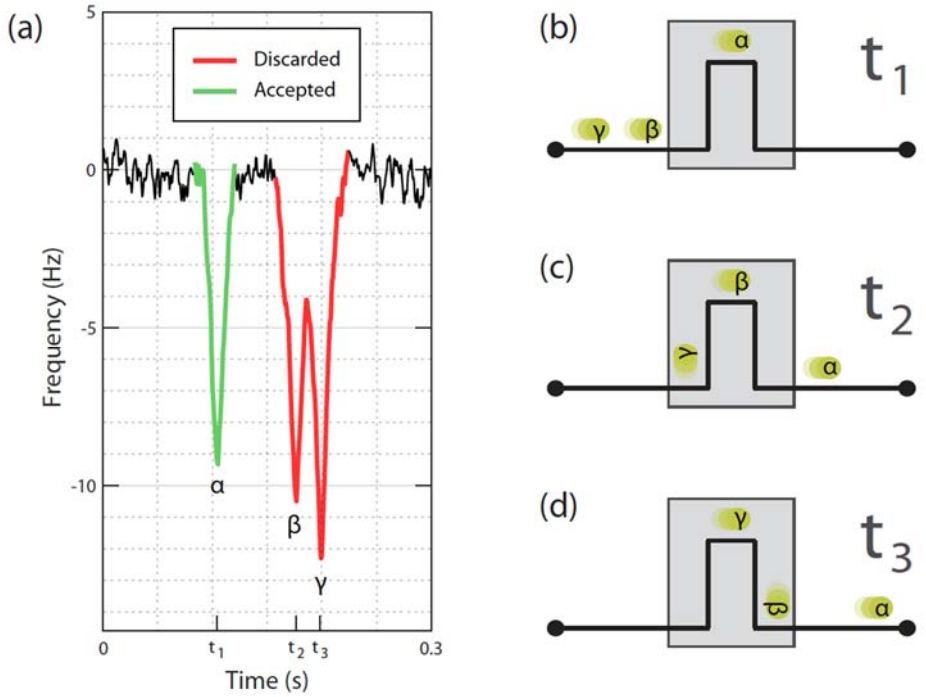

Figure S23. Measurement of multiple particles being simultaneously present inside the cantilever. (a) Resonance frequency shift peaks corresponding to three 40-nm gold nanoparticles (α, β, γ) passing through the SNR channel at different times: t1, t2, t3. While α is being measured, no other particle goes through the SNR and the resulting frequency shift peak is easily detectable by the MATLAB post-processing script. (b) shows particle α reaching the tip of the SNR at time t1, while β and γ are still in the bypass channel. The read peak in (a) corresponds to a double-occupancy event and must be discarded by the MATLAB post-processing script. Particles β and γ are both in the SNR but they reach its tip at times t2 and t3 respectively causing a resonance frequency shift shape with two minima. Schematics (c) and (d) show particles β and γ in the SNR at times t2 and t3, while particle α has already left the device.

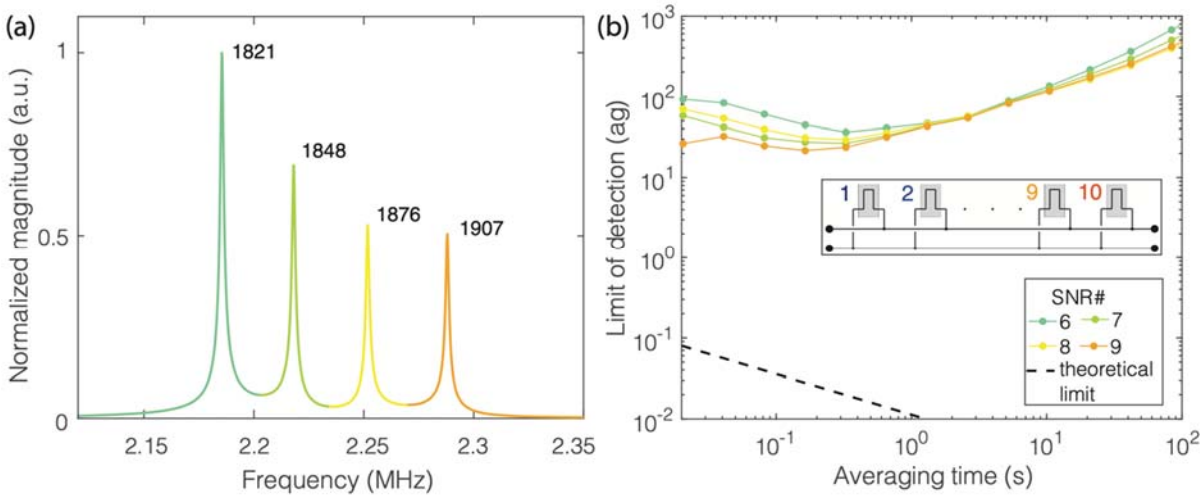

Figure S24. Frequency response (a), and limit of detection of buoyant mass vs averaging time (b) for the A1 SNR array device used for the experiments performed in **Figure 4d,e**. The numbers in black color denote the quality factor of the each one of the four resonators operated in the A1 SNR array. The measurement bandwidth in (b) was set to 150 Hz. The resulting mass-equivalent noise based on the Allan deviation is approximately 20-40 ag. All measurements of (a) and (b) are performed with de-ionized water in the resonators.

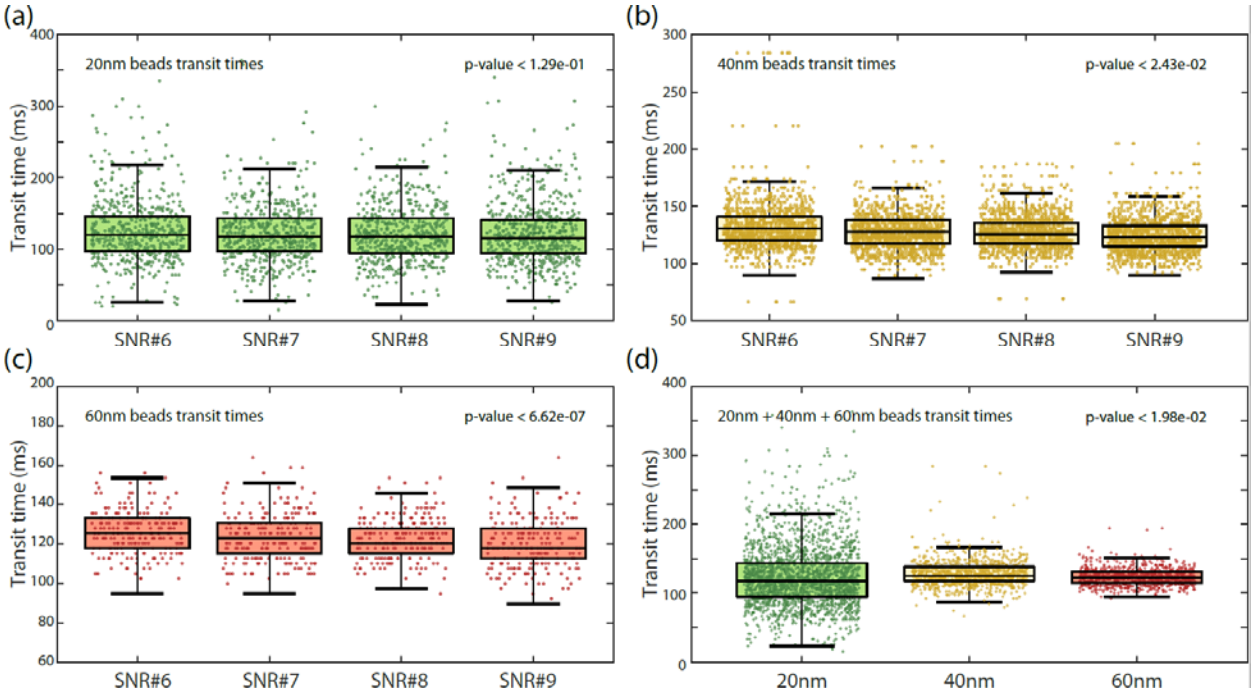

Figure S25. Measurement of transit times for nanoparticles in A1 SNR array. (a, b, c) Transit times of 20 nm (green), 40 nm (yellow), 60 nm (red) gold nanoparticles through an array of 4 SNRs of type A1, as inferred from measurements in **Figure 4d**. The resulting average transit time and corresponding standard deviation are of (123.98 ms, 1.66 ms), (128.36 ms, 0.49 ms) and (122.86 ms, 0.41 ms) for the 20 nm, 40 nm, 60 nm gold nanoparticles respectively. Although the p-values don't allow for the null hypothesis to be discarded, it is reasonable to estimate transit times to be the roughly the same for particles of the same species through 4 different resonators based on their averages and standard deviations. (d) Comparison between transit times grouped according to nanoparticle size. Low p-values don't make it possible to claim that transit times are the same for the different populations, but the low and non-monotonic variation of average transit time with respect to sample size do not allow to claim the opposite either. For clarity, only a tenth of the collected events are plotted in (a-d).

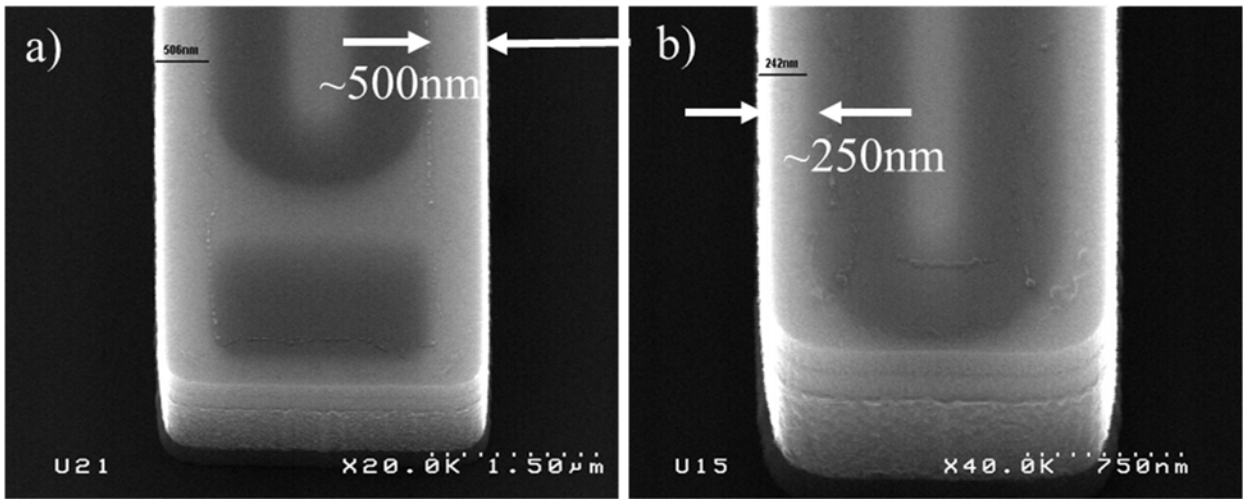

Figure S26. Scanning Electron Microscope images of (a) SNR with conservative wall thickness of 500 nm, and (b) SNR with reduced wall thickness of 250 nm.

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